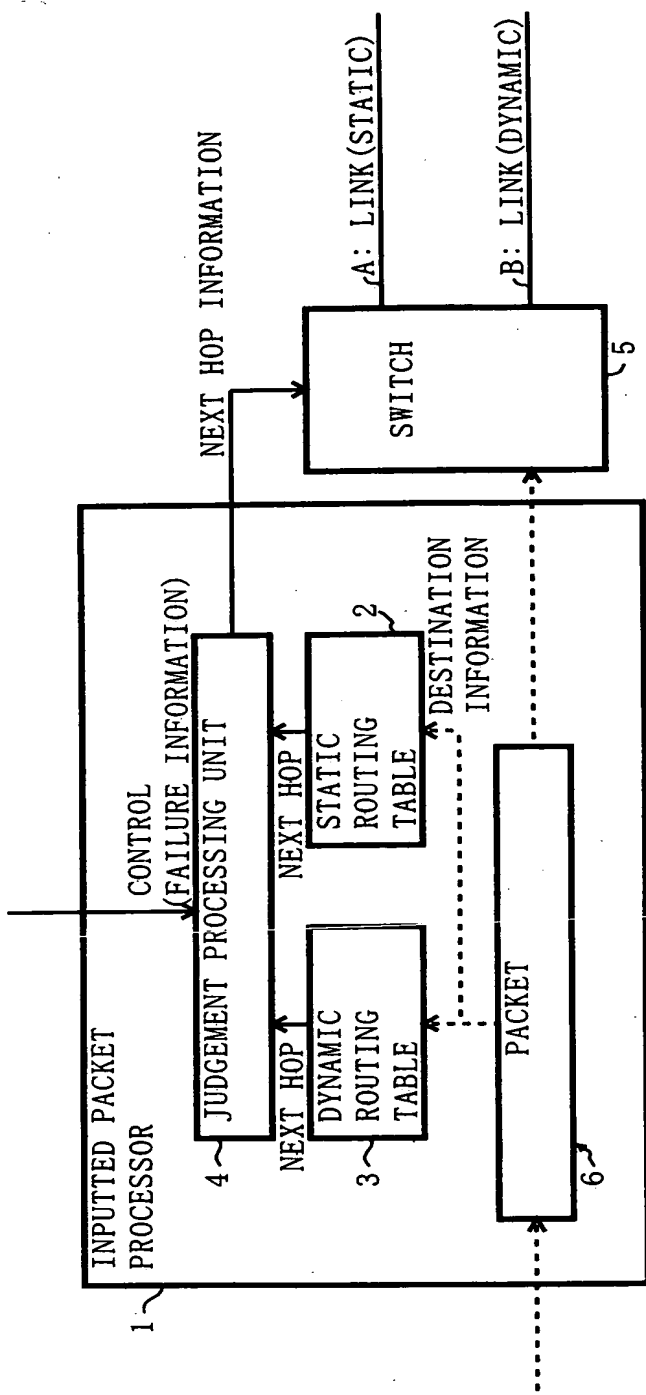


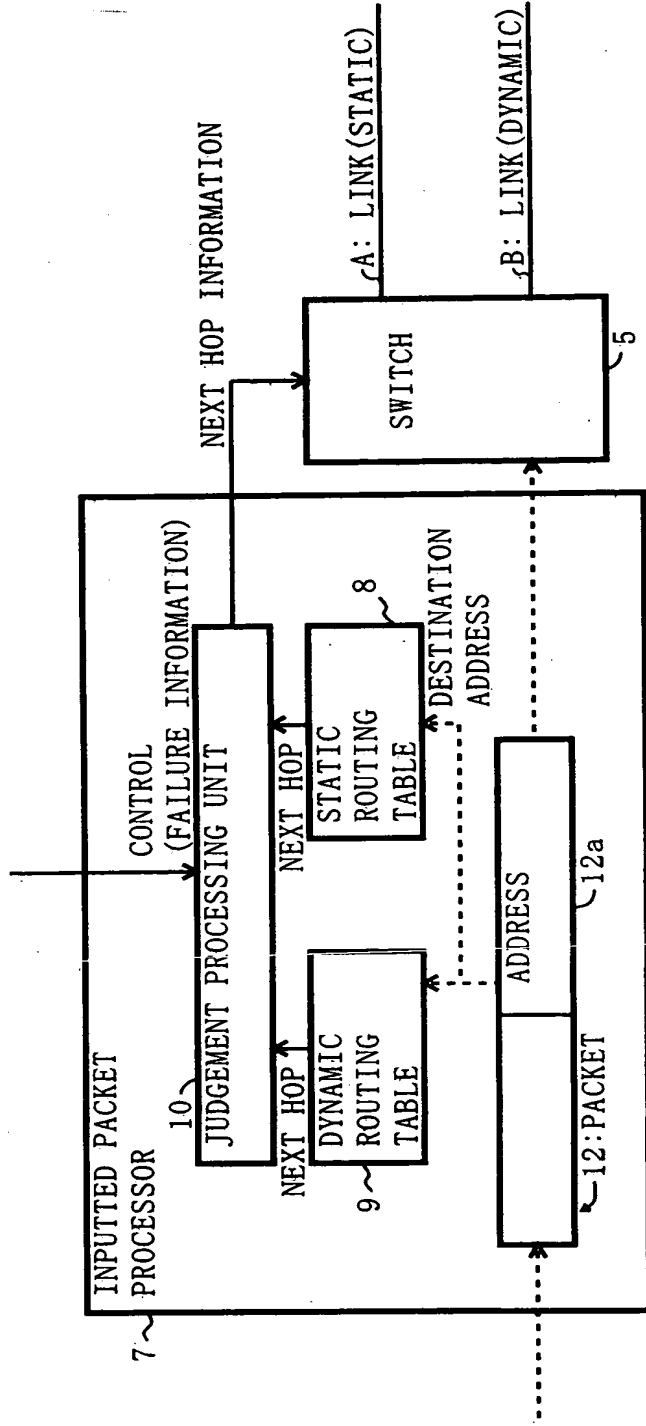


F I G . 1



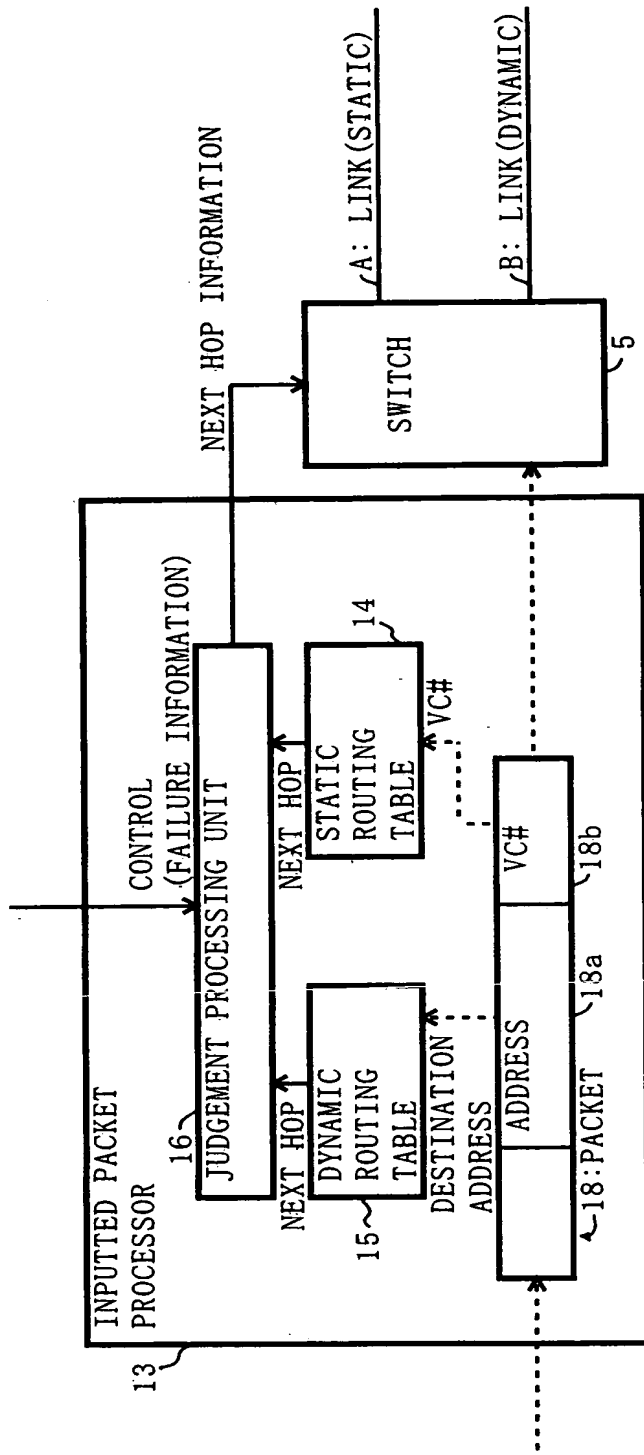


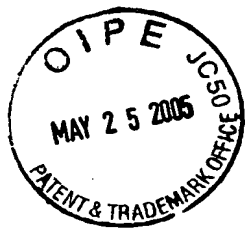
F I G . 2



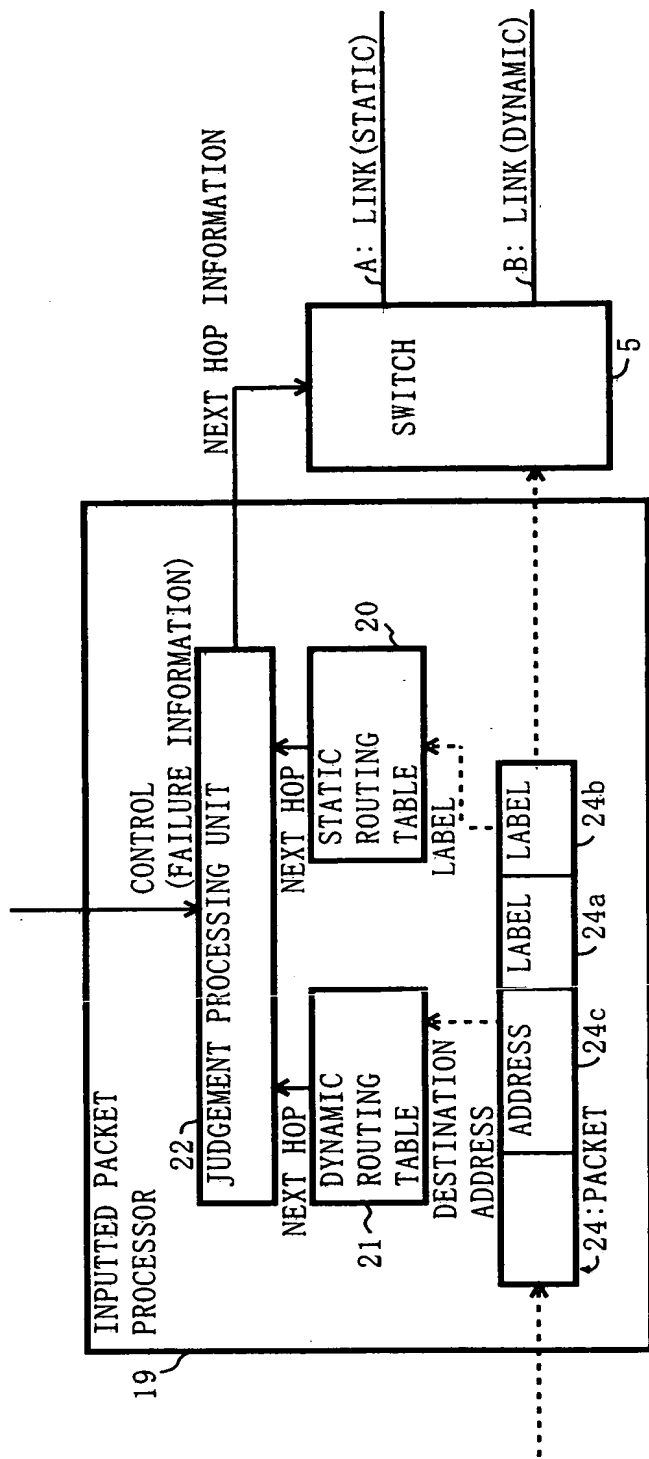


F I G . 3



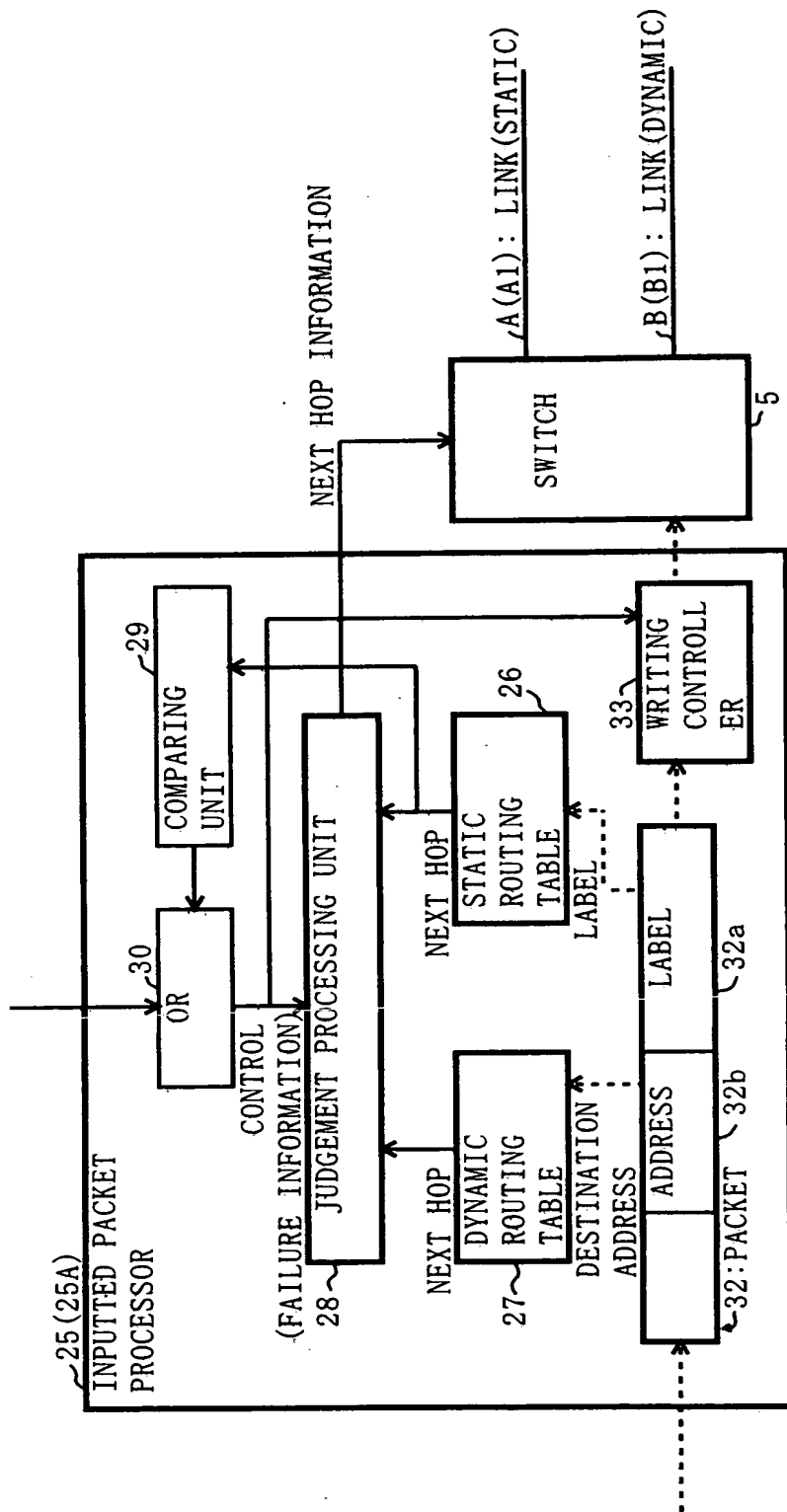


F I G . 4



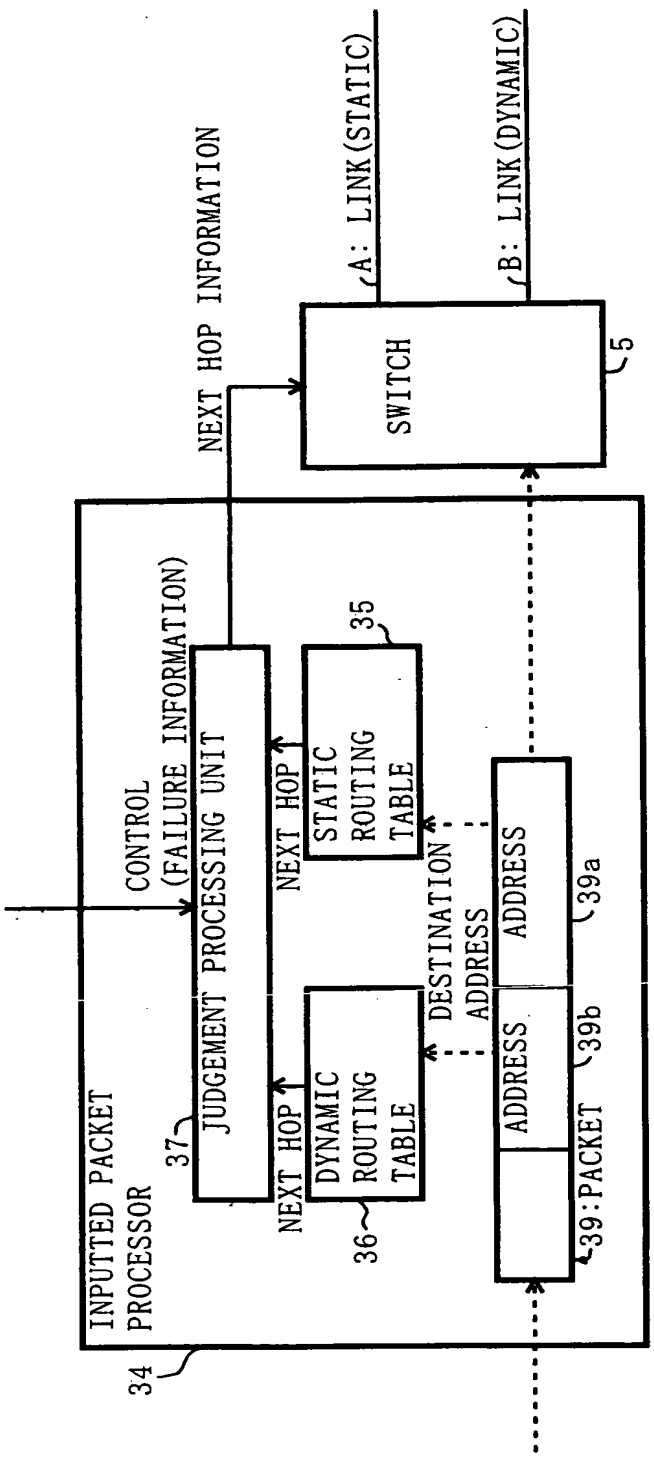


F I G . 5





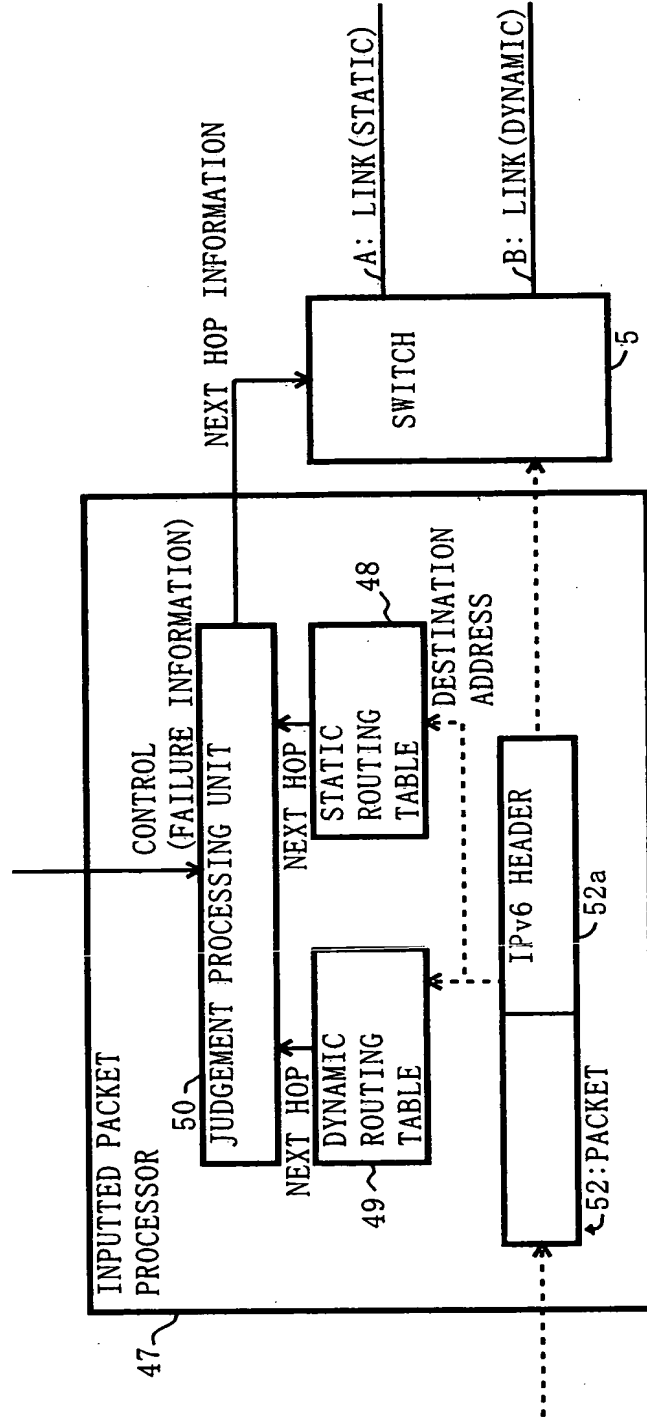
F I G . 6



```

graph LR
    Input[INPUTTED PACKET] --> Processor[40: INPUTTED PACKET PROCESSOR]
    Processor --> Judgement[43: JUDGEMENT PROCESSING UNIT]
    Processor --> Control[44: CONTROL FAILURE INFORMATION]
    Judgement --> NextHopInfo[40: NEXT HOP INFORMATION]
    NextHopInfo --> Switch[5: SWITCH]
    Control --> StaticTable[41: STATIC ROUTING TABLE]
    Control --> DynamicTable[42: DYNAMIC ROUTING TABLE]
    LinkB[40: B: LINK DYNAMIC] --> DynamicTable
    DynamicTable --> DestAddr[40: DESTINATION ADDRESS]
    DestAddr --> StaticTable
    StaticTable --> IPv4Header[45a: IPv4 HEADER]
    IPv4Header --> Packet[45: PACKET]
    Packet --> Switch
  
```

F I G . 9



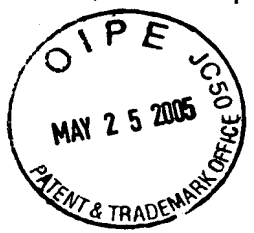


FIG. 11

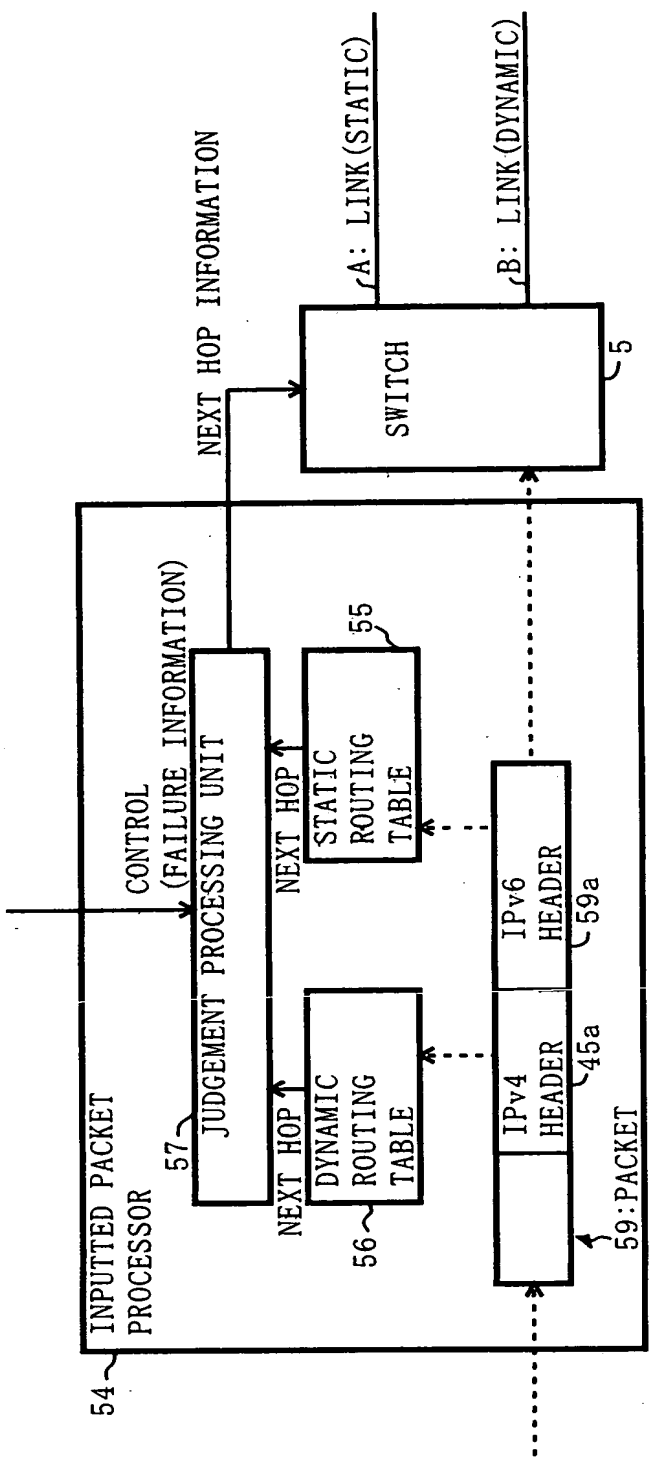
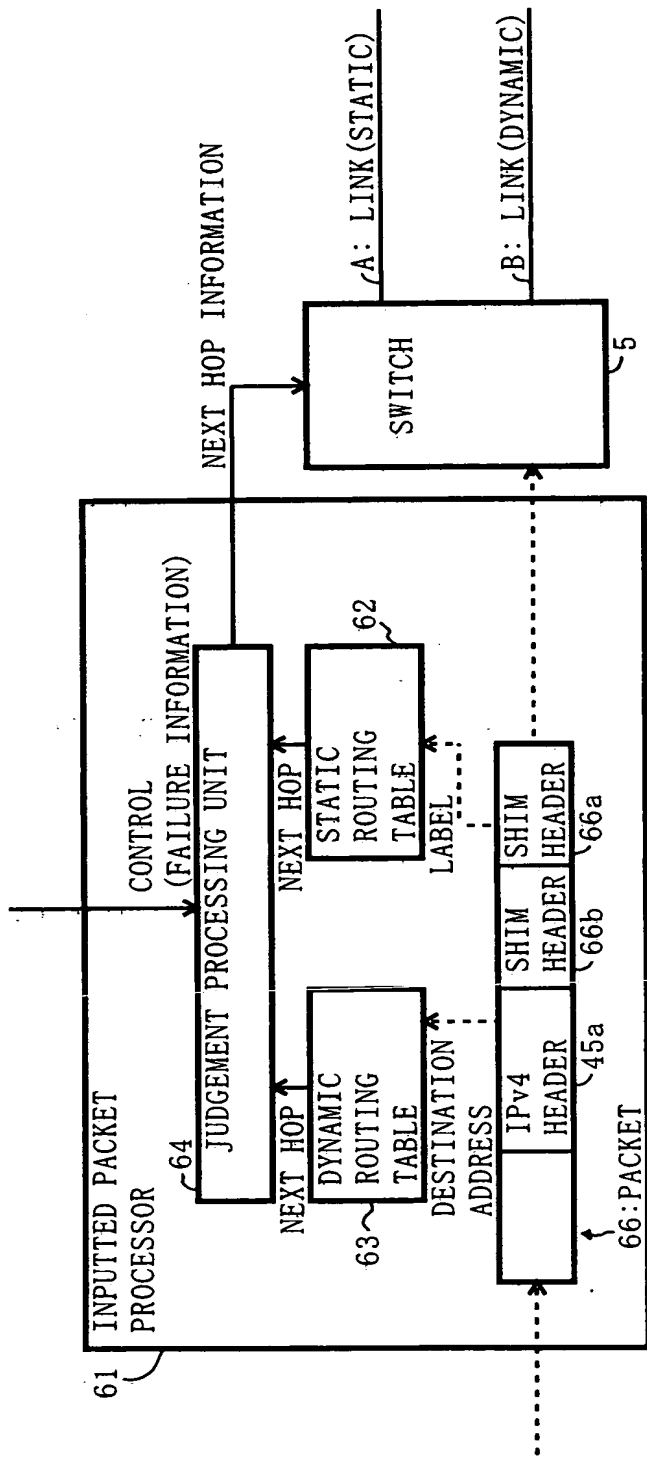


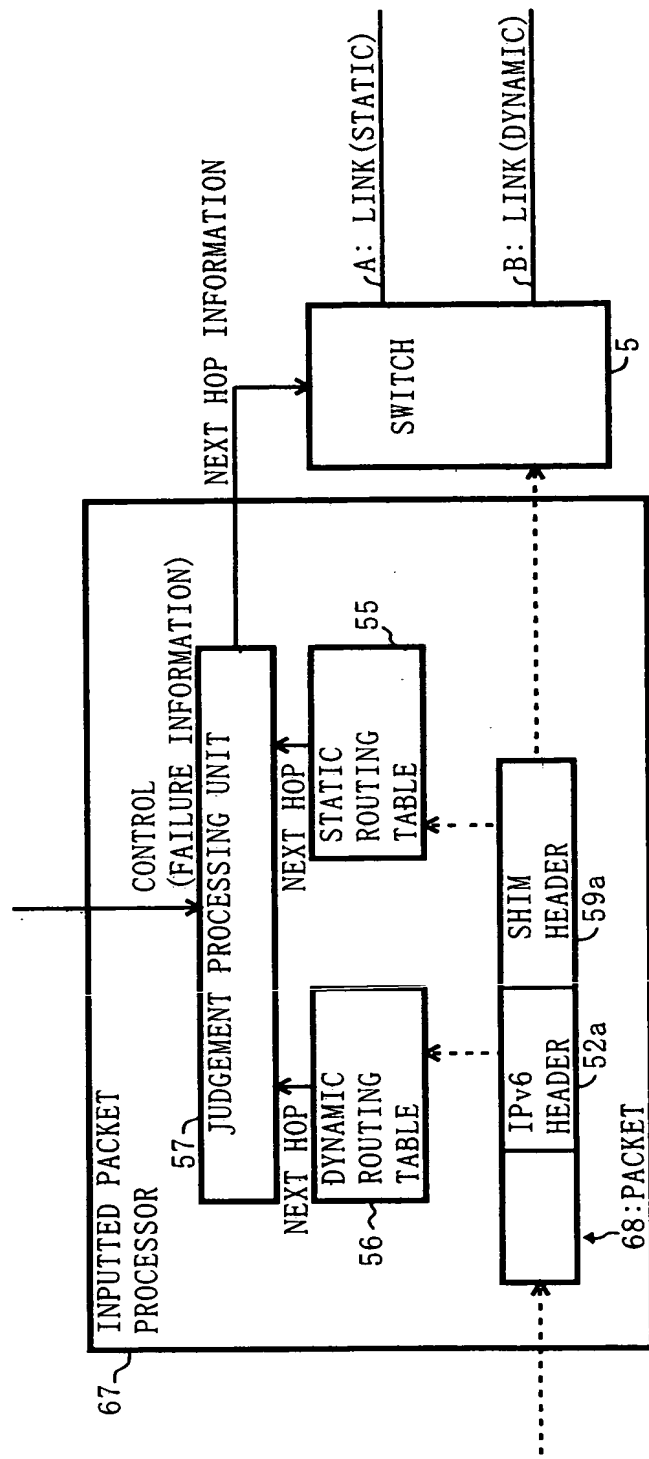


FIG. 13





F I G . 1 4





F I G . 1 5

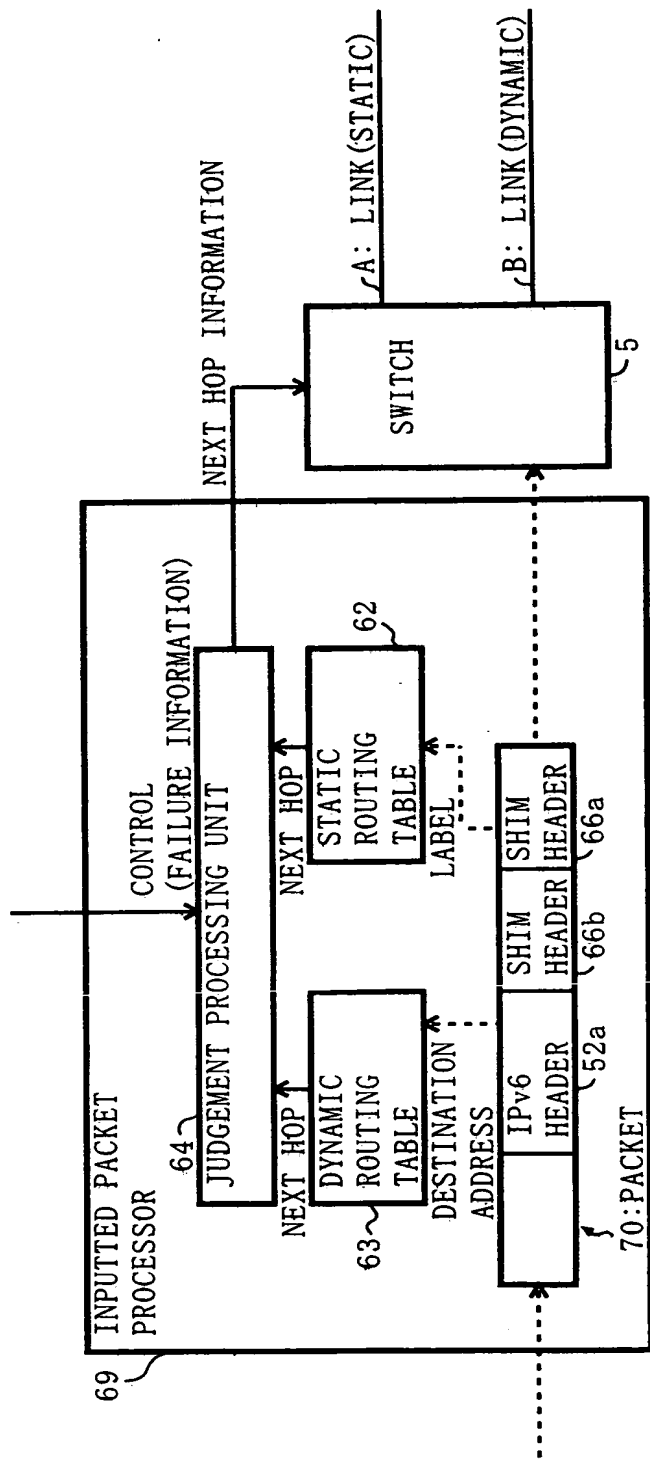
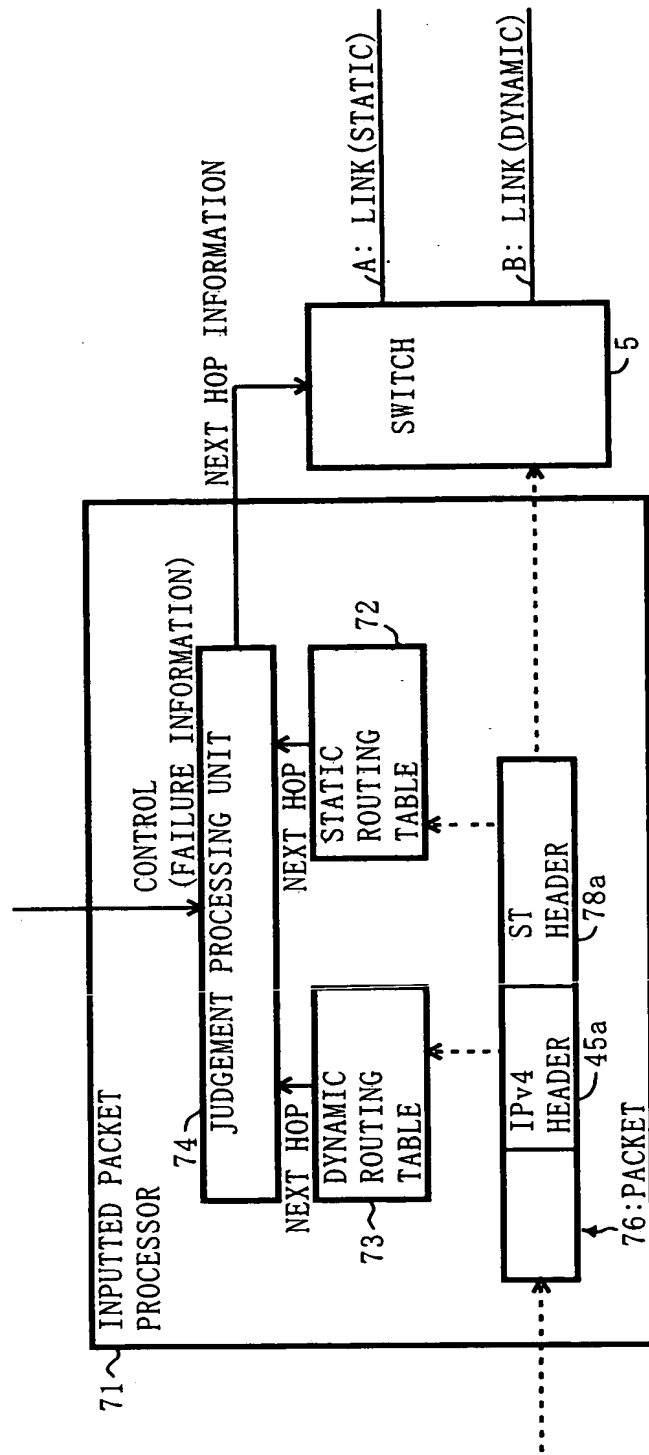




FIG. 16



F I G . 1 8

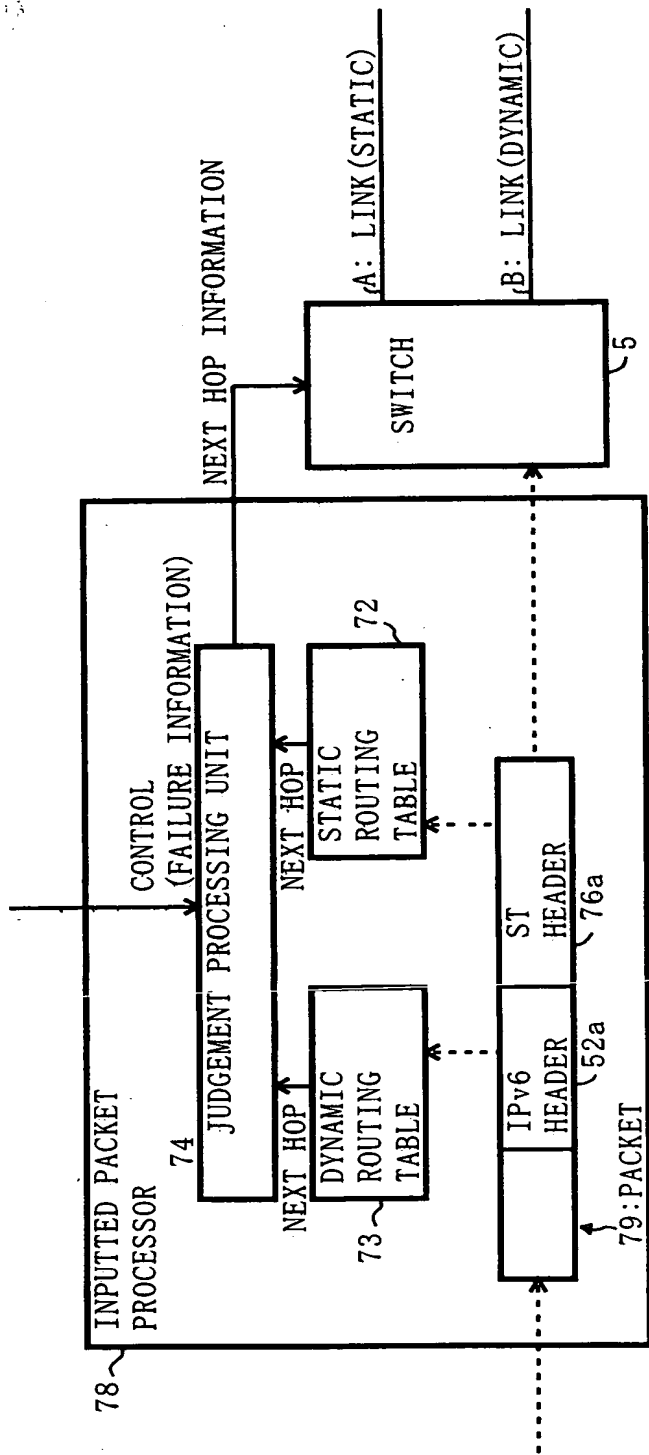
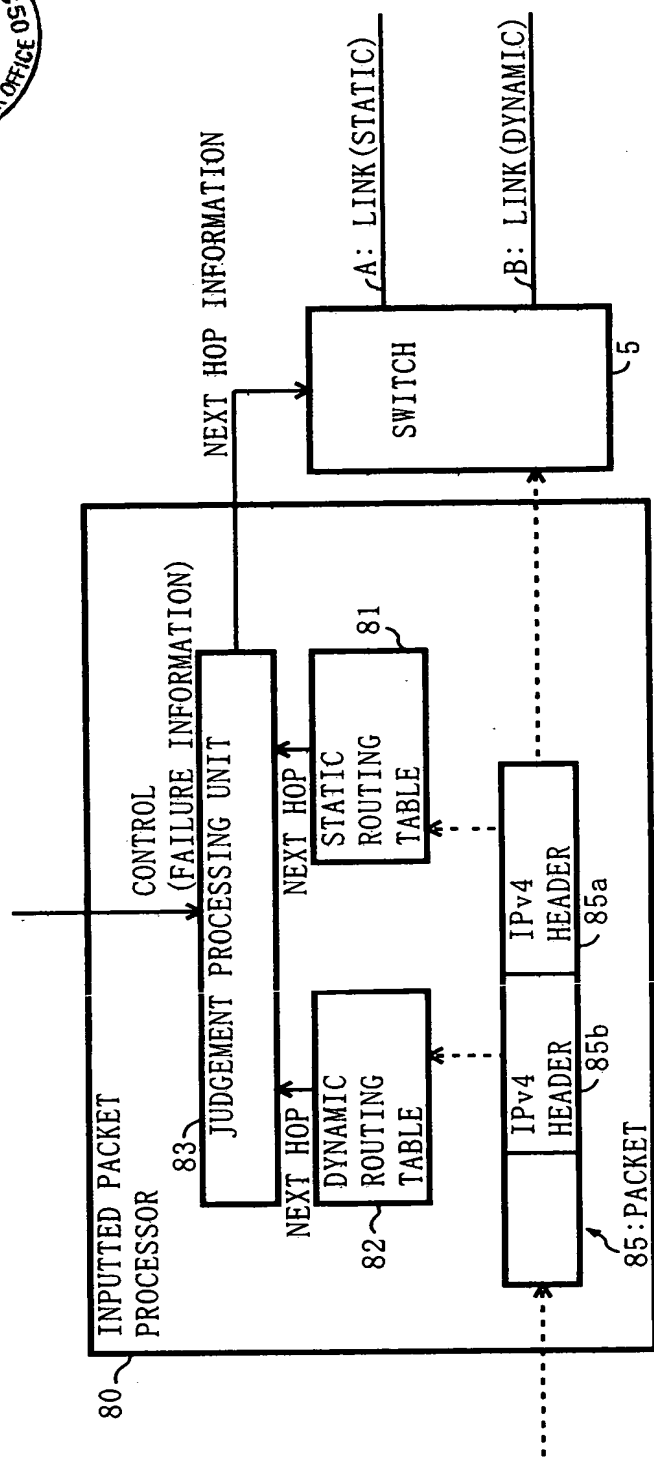
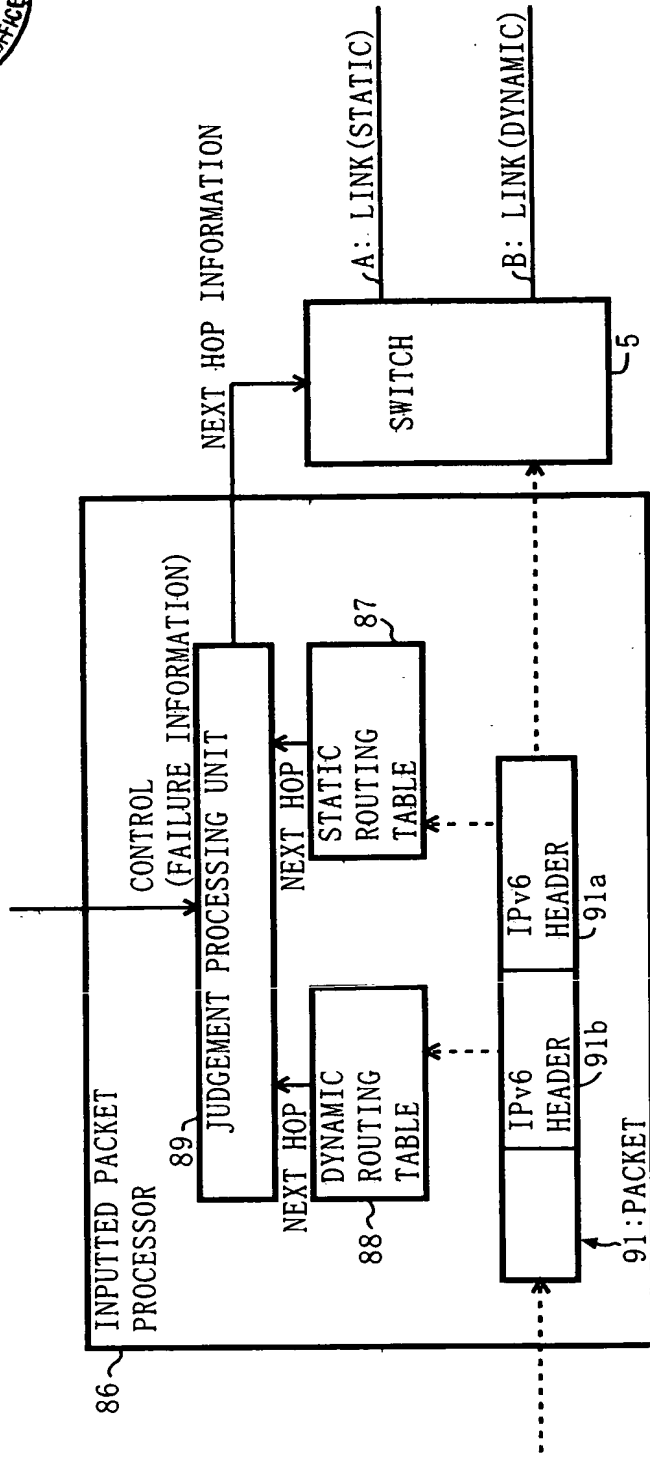


FIG. 19

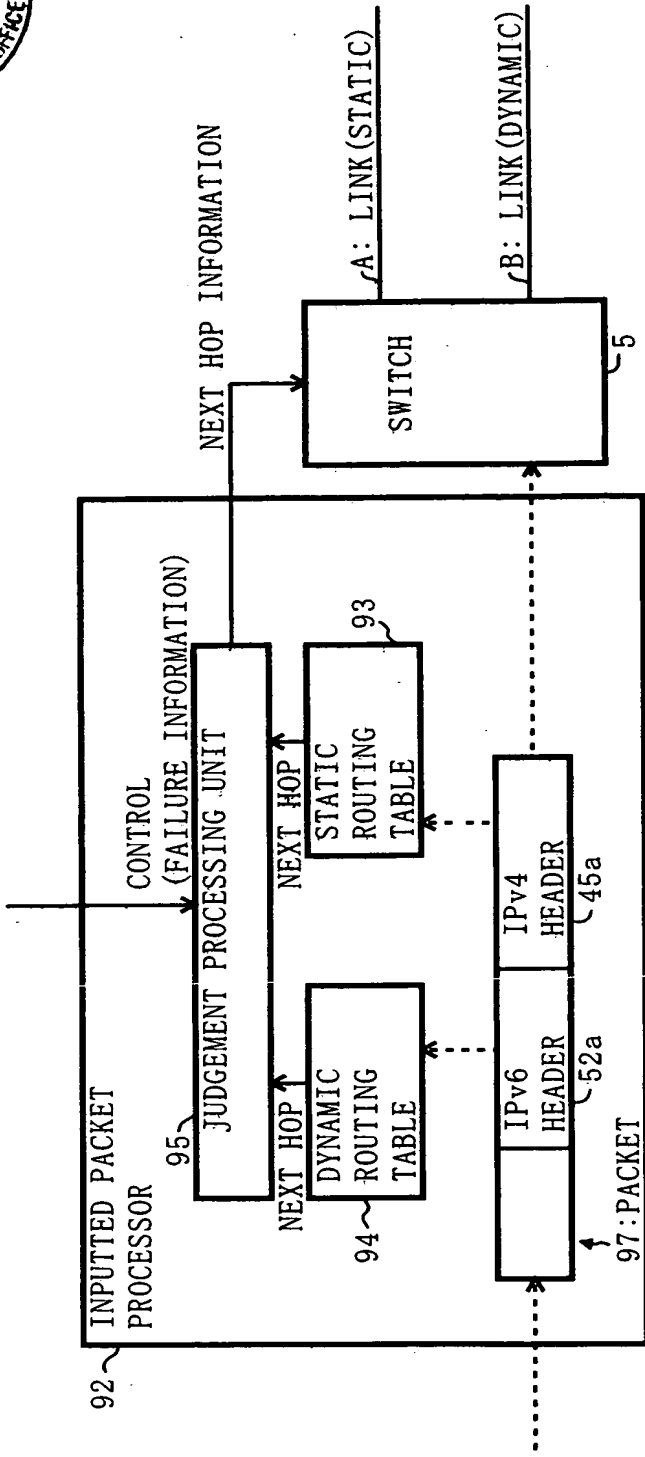




F I G . 2 0

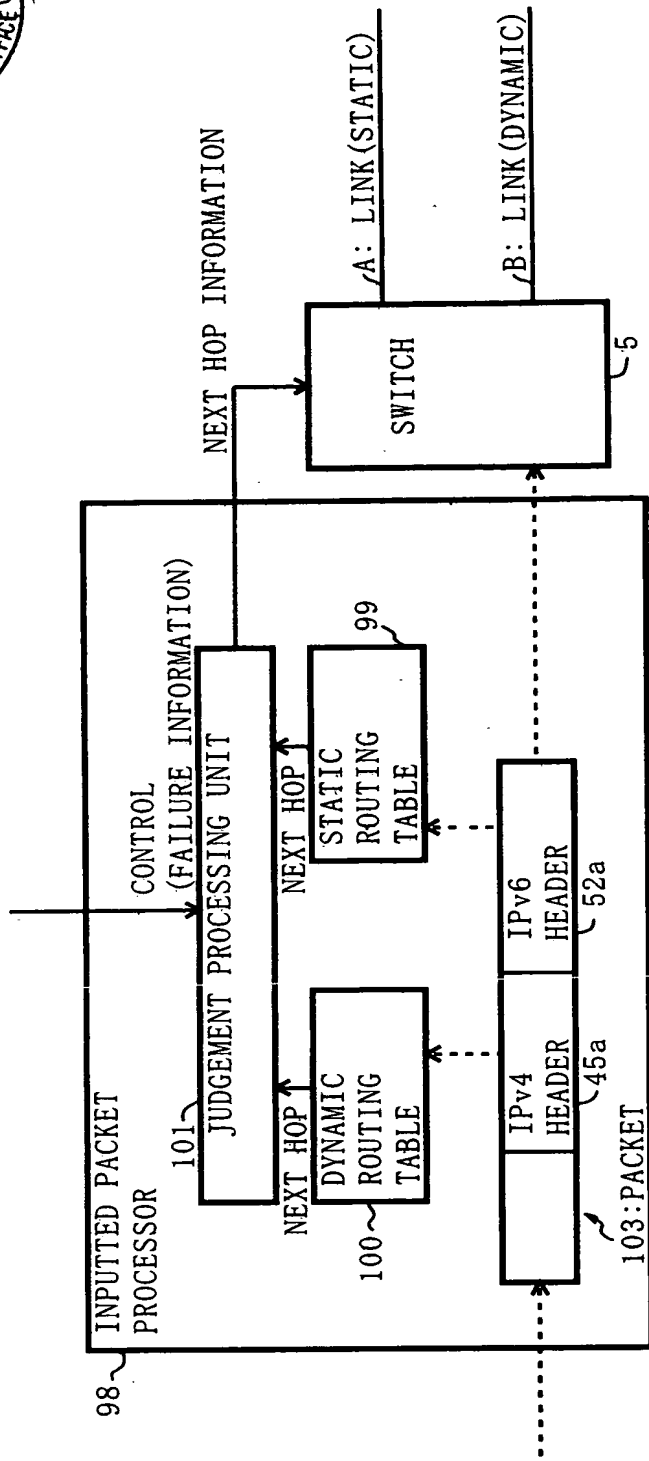


F I G . 2 1





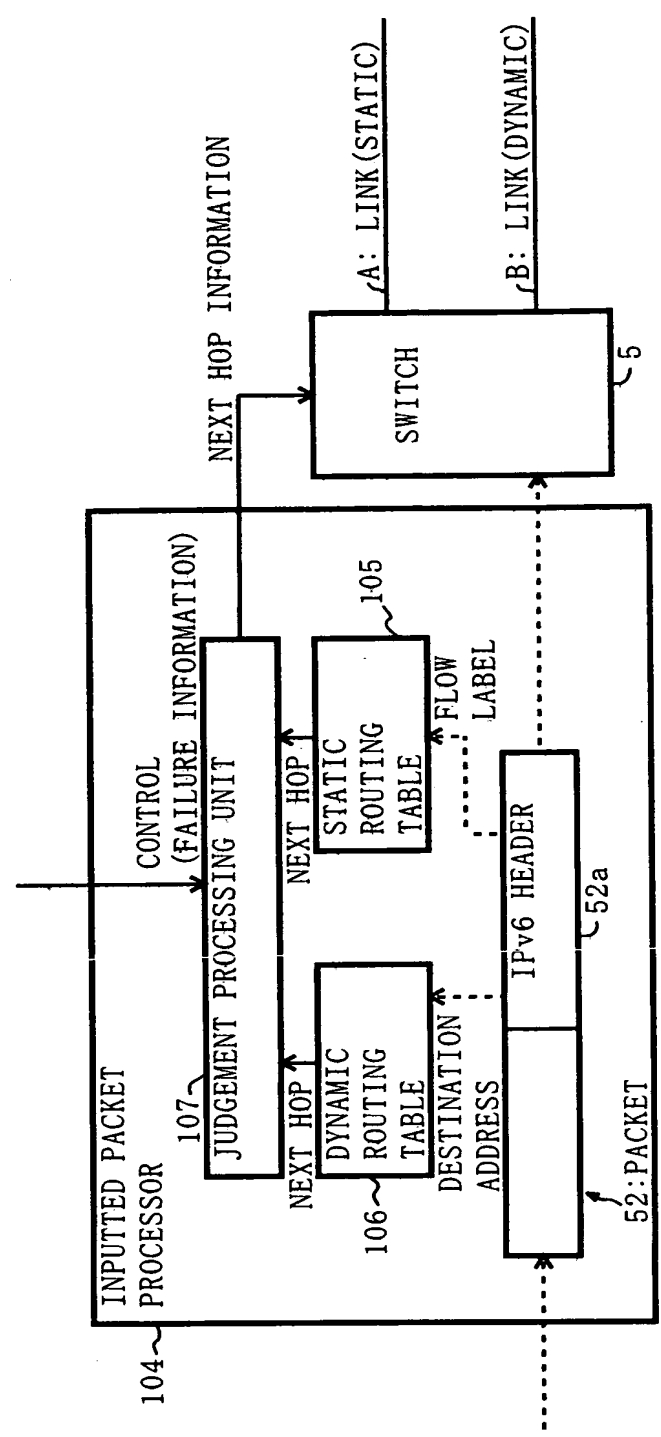
F I G . 2 2



Replacement Sheets

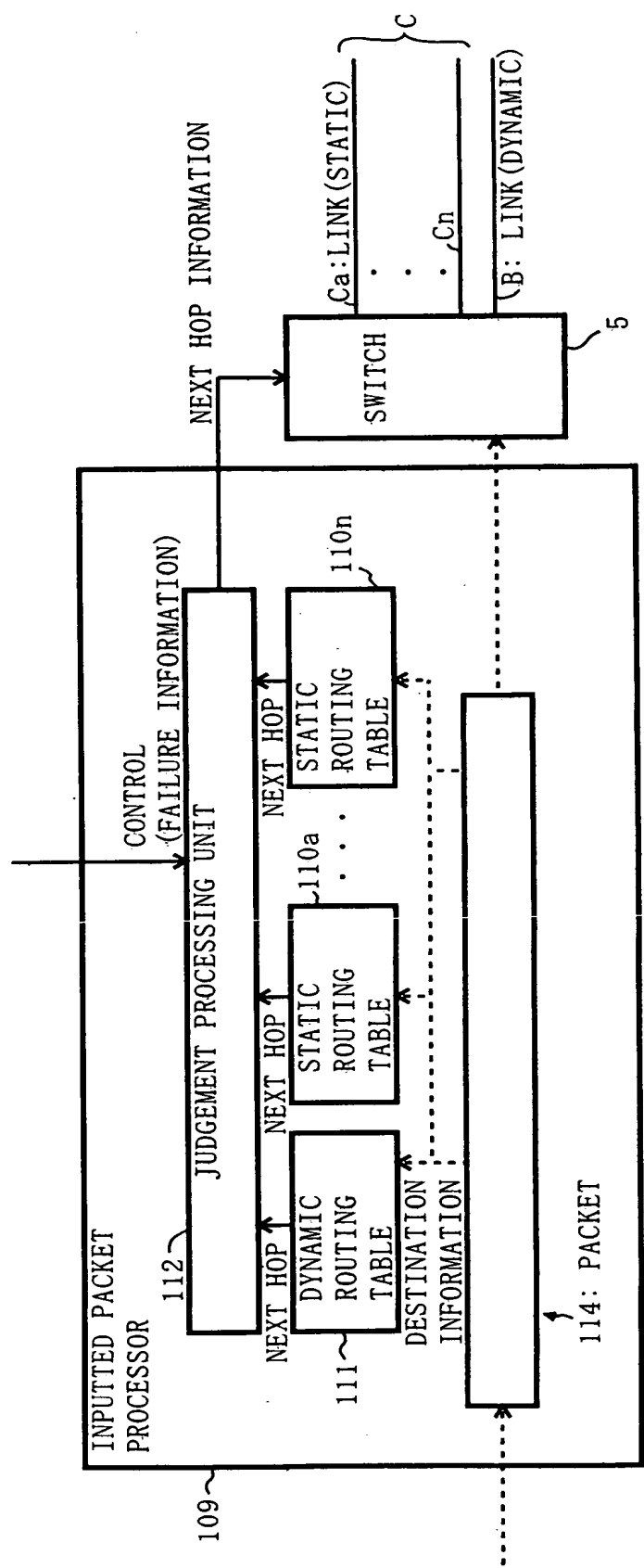


F I G . 2 3





F I G . 2 4





F I G . 2 5

